Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-32 (canceled)

Claim 33. (Previously Presented): A method for block erase of storage sites of a twin MONOS NAND memory array, comprising:

a) applying a high positive voltage to a selected word line,

b) applying a low voltage to unselected word lines,

c) applying a ground potential to a drain of an upper column selector gate,

e) applying a ground potential to a source of a lower column selector,

f) selecting said upper and lower column selectors and erasing both storage sites of each cell in a block of cells.

Claim 34. (Currently Amended) The method for block erase of claim [34] 33, wherein said low voltage is of sufficient magnitude to allow the ground potential to be connected to a source and a drain of each cell in said block of cells through unselected cell in each column containing said block.

Claim 35. (Currently Amended) The method for block erase of claim [34] 33, wherein erasing storage sites is an operation whereby electrons are injected into said storage sites by FN tunneling.

Claim 36. (Previously Presented) A method of programming storage sites in a twin MONOS NAND array, comprising:

a) selecting a first storage site to be programmed of two storage sites contained within a selected memory cell of a column memory cells,

b) connecting a negative voltage to a word gate of said selected memory cell,

c) connecting a positive voltage to a first diffusion extending under said first storage site,

d) connecting a ground potential to a second diffusion extending under a second storage site of said two storage sites,

e) programming said first storage site.

Claim 37. (Presently Amended) The method of programming of claim [37] 36, wherein programming said first storage site is an operation whereby electrons are ejected from said first storage site by FN tunneling or hole injection.

Claim 38. (Presently Amended) The method of programming of claim [37] 36, wherein connecting said positive voltage to said first diffusion further comprises:

a) connecting said positive voltage from a column selector gate by selecting said selector gate,

b) connecting a word line voltage higher in value than said positive voltage to unselected word gates in said column between said column selector gate and said first diffusion.

Claim 39. (Presently Amended) The method of programming of claim [37] 36, wherein connecting said ground potential to said second diffusion further comprises:

a) connecting said ground potential from a column selector gate by selecting said selector gate,

b) connecting a word line voltage higher in value than said ground potential to unselected word gates in said column between said column selector gate and said second diffusion.

Claim 40. (Previously Presented) A method of reading storage sites in a twin MONOS NAND array, comprising:

a) selecting a first storage site to be read from two storage sites contained within a selected memory cell of a column memory cells,

b) connecting a first positive voltage to a word gate of said selected memory cell,

c) connecting a ground potential to a first diffusion extending under said first storage site to be read,

c) connecting a second positive voltage to a second diffusion extending under a second storage site not being read,

e) reading a current when the word gate voltage becomes higher than cell thresh hold voltage depending upon the data stored in said first storage site.

Claim 41. (Presently Amended) The method of reading storage sites of claim [41] 40, wherein said first positive voltage is a value near a programmed threshold voltage of said memory cell.

Claim 42. (Presently Amended) The method of reading storage sites of claim [41] 40, wherein said second positive voltage is less than said first positive voltage.

Claim 43. (Presently Amended) The method of reading storage sites of claim [41] 40, wherein connecting said ground potential to said first diffusion further comprises:

a) selecting a column selector gate connecting said ground potential to said column,

b) applying a positive voltage to word lines of unselected memory cells between said column selector and said first diffusion.

Claim 44. (Presently Amended) The method of reading storage sites of claim [41] 40, wherein connecting said second positive voltage to said second diffusion further comprises:

a) selecting a column selector gate connecting said second positive voltage to said column,

b) applying a positive voltage to word lines of unselected memory cells between said column selector and said second diffusion.

Claim 45. (Presently Amended) The method of reading storage sites of claim [41] 40 further comprising:

a) said second positive voltage connected to said second diffusion produces a low threshold voltage for said second storage site,

b) said first storage site has a high threshold voltage when charged with electrons representing said first storage site not being programmed thereby blocking a flow of current,

c) said first storage site has said low threshold voltage when not charged with electrons representing said first storage site being programmed thereby allowing said flow of current,

d) said flow of current indicates a stored data value in said first storage site.

Claims 46-61 (Cancelled)